Achieving Sustainable SIMD Performance for High Order DG Methods through Code Generation

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Abstract: Explicit SIMD vectorization is one of the key challenges in achieving good floating point performance on modern HPC platforms. Typically, compiler-based auto-vectorization is only applicable if the problem exhibits a favorable structure. However, domain knowledge may be used to identify alternate sources of parallelism to be used for SIMD vectorization at the cost of writing code, that is tuned specifically to the PDE problem at hand and to the target architecture. We solve the maintainability issue of such codes through a code generation approach: Explicitly vectorized finite element assembly kernels to be used with the discretization framework dune-pdelab are generated from a DSL (UFL) describing the finite element assembly problem. We demonstrate the power and flexibility of the approach for high order DG methods on hexahedra, exploiting the tensor product structure of basis functions and quadrature formulas through sum factorization. Performance numbers on the latest Intel architectures Haswell, Xeon Phi and Skylake are shown.

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