Future Directions in High Performance Computing (HPC) 2009 - 2018

Horst D. Simon[1]

Abstract: Since about 2004 there has been a fundamental transition taking place in computing. The microprocessors clock speed improvement have leveled off, and future performance increases from processors will be realized through multi-core and many-core chips. This change in the basic building blocks for HPC has opened up the architecture discussion for future HPC platforms, and in 2008 we see vigorous experimentation with accelerators, GPUs, FPGAs, and embedded technology. HPC has not seen such a variety of new technology being explored since the early 1990s. In my talk I will explore what the multi-core revolution will mean for the future of HPC. I will use the very successful model of the HPC ecosystem and its important elements economic driver, system architecture, and programming model to explain how I think HPC will develop in the next five years. Several of the projects that are currently going on in Berkeley will be discussed in detail, since they will provide tools for the future productive use of supercomputers. They include auto-tuning, PGAS languages, and most importantly the Green Flash project, that attempts to find a new solution for energy efficient computing in the future.

[1] Associate Laboratory Director, Computing Sciences Mail Stop 50B 4230
Lawrence Berkeley National Laboratory
Berkeley, CA 94720, USA
and
Adjunct Professor
Electrical Engineering and Computer Science (EECS) Department
University of California
Berkeley, CA 94720, USA
hdsimon@lbl.gov