Layout Improvement for the Facility Design of Semiconductor Fabrication

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Abstract: Several layout improvement heuristics are proposed to reduce the wafer transportation distance for spine bay fab design. These heuristics can reach near-optimal fab design in reasonable computational time. Among these heuristics, the one combining Threshold Accepting and Steepest Descent Plus leads to the best performance.

Better facility planning of wafer fabs leads to a higher productivity, shorter wafer move distance, higher machine utilization, higher fab space utilization, and better competitiveness. A spine bay configuration arranges bays along a central spine. This is a typical design of modern fabs manufacturing 8-inch and 12-inch semiconductor wafers. In this design, equipment (i.e., tools) of the same type are allocated to the same bay and an interbay material handling system (IMHS) is located at the spine area. After been processed at one bay, a wafer is transported by the IMHS to another bay for next processing. This continues until the wafer's entire production steps are processed. The spine bay design results in low transportation cost and an efficient flow.

This research proposes and evaluates five layout improvement heuristics for spine bay fab design: Two-Phase, Steepest Descent, Steepest Descent Plus (SDP), Threshold Accepting (TA) and Hybrid. Hybrid heuristics combines SDP and TA and adopts space-filling concept to manage traditional space constraints. This heuristics first uses SDP to search local solutions and then uses TA to jump out from local optimal and continue to search better solutions. All these five heuristics can be used to reduce the wafer transportation distance by changing the location of the bays, after an initial fab design is generated.

These layout improvement heuristics are evaluated on the basis of several fab designs with 8 to 20 bays. Three typical wafer products with an average of 200 production steps are taken into account. SDP, TA, and Hybrid heuristics lead to better solutions than the others. The quality of solution is better than 96% of the optimal one. However, the required computational time using these heuristics is much less than the enumeration method when the number of bays increases. Among these three heuristics, Hybrid has the lowest solution variation.

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